IN THE CLAIMS

Please cancel claims 11 and 27, and amend the remaining claims to read as indicated herein.

1. (currently amended) An automated computer-implemented method ~~for a pre-layout estimation of a characteristic of a standard cell, said method~~ comprising:

receiving a pre-layout representation of ~~said~~ a standard cell;

applying ~~at least one~~ a transformation to said pre-layout representation to obtain an estimated ~~representation~~ value of a parasitic of said standard cell; and

~~characterizing said estimated representation to obtain said pre-layout estimation of said characteristic of said standard cell~~

estimating a value for a characteristic of said standard cell, based on said estimated value of said parasitic.

2. (original) The method of claim 1, wherein said pre-layout representation is selected from the group consisting of: a spice netlist, a BDD-based transistor structure representation, and a pre-layout structural representation.

3. (currently amended) The method of claim 1, ~~wherein a statistical pre-layout estimator is used to obtain said pre-layout estimation of said standard cell~~ wherein said estimating is further based on a representative set of laid out cells for a particular technology and cell architecture.

4. (currently amended) The method of claim ~~3~~ 1, wherein said ~~statistical pre-layout estimation of said standard cell~~ estimating is accurate to within about 5 percent of a post-layout ~~timing characterization of a parasitic-dependent timing characteristic of~~ value of said characteristic for said standard cell.

5. (currently amended) The method of claim 1, wherein ~~a constructive estimator obtains said pre-layout estimation of said standard cell that~~ said estimating is accurate to within about 1.5 percent of a post-layout ~~timing characterization of a parasitic-dependent timing characteristic of~~ value of said characteristic for said standard cell.

6. (currently amended) The method of claim 1, wherein said characteristic ~~comprises~~ is a parasitic-dependent standard cell characteristic.

7. (currently amended) The method of claim ~~6~~ 1, wherein said ~~parasitic-dependent standard cell~~ characteristic is selected from the group ~~of standard cell characteristics~~ consisting of: timing, power, input capacitance, and noise~~, and any other parasitic-dependent standard cell characteristic~~.

8. (currently amended) The method of claim 1, wherein said ~~at least one~~ transformation is selected from the group consisting of: transistor folding, diffusion area and perimeter assigning of transistors of said standard cell, and adding wiring capacitances to said pre-layout representation.

9. (original) The method of claim 8, wherein said transistor folding transformation is performed prior to said diffusion area and perimeter assigning of transistors of said standard cell transformation, and adding wiring capacitances to said pre-layout representation.

10. (currently amended) The method of claim 1, wherein said ~~at least one~~ transformation comprises assigning a diffusion area and a perimeter to transistors of said standard cell, wherein a diffusion region width, w, is estimated as $S_{pp}/2$ ~~in the instance~~ for a case in which a net associated with said diffusion region is an intra-MTS net, and w is estimated as $W_c/2 + S_{pc}$ ~~in the instance~~ for a case in which a net associated with said diffusion region is an inter-MTS net, wherein Spp is a minimum poly-to-poly spacing, W_c is a contact width, and S_{pc} is a minimum poly-to-poly spacing.

11. (canceled)

12. (currently amended) The method of claim 1, wherein said pre-layout representation is a pre-layout netlist and said ~~at least one~~ transformation comprises adding a wiring capacitance to each net in said pre-layout netlist, and a capacitance C(n) of a net n is estimated as:

$$C(n) = \alpha \sum_{t \in TDS(n)} |MTS(t)| + \beta \sum_{t \in TG(n)} |MTS(t)| + \gamma$$

wherein α, β and γ are constants, *TDS(n)* is a set of transistors whose drain or source is connected to a net n, *TG(n)* is a set of transistors whose gate is connected to said ~~net *n* and~~ net *n*, *MTS(t)* is ~~an MTS (Maximal Transistor Series)~~ a maximal transistor series that includes a transistor *t*, and *|MTS(t)|* is a number of transistors in *MTS(t)*.

13. (currently amended) The method of claim 12, wherein said constants α, β and γ are predetermined prior to said application of said ~~at least one~~ transformation to said pre-layout representation.

14. (original) The method of claim 12, wherein said constants α, β and γ are determined by multiple regression analysis based on a representative set of laid out cells for a particular technology and cell architecture.

15. (currently amended) The method of claim 1, wherein said characteristic ~~comprises~~ is a parasitic-dependent timing characteristic of said standard ~~cell~~ cell, and said ~~at least one~~ transformation comprises diffusion area and perimeter assigning of transistors of said standard cell, and adding wiring capacitances to said pre-layout representation.

16. (original) The method of claim 1, wherein said characteristic is selected from the group consisting of: a cell footprint and a pin placement of said cell.

17. (currently amended) A storage medium including computer readable program instructions for an automated computer-implemented method ~~for obtaining a pre-layout estimation of a characteristic of a standard cell~~, said storage medium comprising:

program instructions for receiving a pre-layout representation of a standard cell;

program instructions for applying ~~at least one~~ a transformation to said pre-layout representation to obtain an estimated ~~representation~~ value of a parasitic of said standard cell; and

~~program instructions for characterizing said estimated representation to obtain said pre-layout estimation of said characteristic of said standard cell~~

program instructions for estimating a value for a characteristic of said standard cell, based on said estimated value of said parasitic.

18. (original) The storage medium of claim 17, wherein said pre-layout representation is selected from the group consisting of: a spice netlist, a BDD-based transistor structure representation, and a pre-layout structural representation.

19. (currently amended) The storage medium of claim 17, ~~further comprising program instructions for a statistical estimator to obtain said pre-layout estimation of said standard cell~~ wherein said estimating is further based on a statistical analysis of differences between pre-layout operation and post-layout operation of a set of standard cells.

20. (currently amended) The storage medium of claim ~~19~~ 17, wherein said ~~statistical pre-layout estimation of said standard cell~~ estimating is accurate to within about 5 percent of a post-layout ~~timing characterization of a parasitic-dependent timing characteristic of~~ value of said characteristic for said standard cell.

21. (currently amended) The storage medium of claim 17, wherein ~~a constructive estimator obtains a pre-layout estimation of said standard cell that~~ said estimating is accurate to

within about 1.5 percent of a post-layout ~~timing characterization of a parasitic-dependent timing characteristic of~~ value of said characteristic for said standard cell.

22. (currently amended) The storage medium of claim 17, wherein said characteristic ~~comprises~~ is a parasitic-dependent standard cell characteristic.

23. (currently amended) The storage medium of claim ~~22~~ 17, wherein said ~~parasitic-dependent standard cell~~ characteristic is selected from the group ~~of standard cell characteristics~~ consisting of: timing, power, input capacitance, and noise~~, and any other parasitic-dependent standard cell characteristic~~.

24. (currently amended) The storage medium of claim ~~16~~ 17, wherein said ~~at least one~~ transformation is selected from the group consisting of: transistor folding, diffusion area and perimeter assigning of transistors of said standard cell, and adding wiring capacitances to said pre-layout representation.

25. (original) The storage medium of claim 24, wherein said transistor folding transformation is performed, per program instructions, prior to said diffusion area and perimeter assigning of transistors of said standard cell transformation, and adding wiring capacitances to said pre-layout representation.

26. (currently amended) The storage medium of claim 17, wherein said ~~at least one~~ transformation comprises assigning a diffusion area and a perimeter to transistors of said standard cell, wherein a diffusion region width, w, is estimated as $S_{pp}/2$ ~~in the instance~~ for a case in which a net associated with said diffusion region is an intra-MTS net, and w is estimated as $W_c/2 + S_{pc}$ ~~in the instance~~ for a case in which a net associated with said diffusion region is an inter-MTS net, wherein Spp is a minimum poly-to-poly spacing, W_c is a contact width, and S_{pc} is a minimum poly-to-poly spacing.

27. (canceled)

28. (currently amended) The storage medium of claim 17, wherein said pre-layout representation is a pre-layout netlist and said ~~at least one~~ transformation comprises adding a wiring capacitance to each net in said pre-layout netlist, and a capacitance C(n) of a net n is estimated as:

$$C(n) = \alpha \sum_{t \in TDS(n)} |MTS(t)| + \beta \sum_{t \in TG(n)} |MTS(t)| + \gamma$$

wherein α, β and γ are constants, *TDS(n)* is a set of transistors whose drain or source is connected to a net n, *TG(n)* is a set of transistors whose gate is connected to said ~~net *n* and~~ net *n*, *MTS(t)* is ~~an MTS (Maximal Transistor Series)~~ a maximal transistor series that includes a transistor *t*, and *|MTS(t)|* is a number of transistors in *MTS(t)*.

29. (currently amended) The storage medium of claim 28, wherein said constants α, β and γ are predetermined prior to said application of said ~~at least one~~ transformation to said pre-layout representation.

30. (original) The storage medium of claim 28, wherein said constants α, β and γ are determined by multiple regression analysis based on a representative set of laid out cells for a particular technology and cell architecture.

31. (currently amended) The storage medium of claim 17, wherein said characteristic ~~comprises~~ is a parasitic-dependent timing characteristic of said standard ~~cell~~ cell, and said ~~at least one~~ transformation comprises diffusion area and perimeter assigning of transistors of said standard cell, and adding wiring capacitances to said pre-layout representation.

32. (original) The storage medium of claim 17, wherein said characteristic is selected from the group consisting of: a cell footprint and a pin placement of said cell.